ABSTRACT

A withstand voltage against electrostatic discharge of a high voltage MOS transistor is improved. An N^--type drain layer is not formed under an N^+-type drain layer, while a P^+-type buried layer is formed in a region under the N^+-type drain layer. A PN junction of high impurity concentration is formed between the N^+-type drain layer and the P^+-type buried layer. In other words, a region having low junction breakdown voltage is formed locally. The surge current flows through the PN junction into the silicon substrate before the N^--type drain layer below a gate electrode is thermally damaged. Hence, the ESD withstand voltage is improved.